IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Fernando Gonzalez et al.	§	Group Art Unit: 2815
Prior Application Serial No.: 09/570,614	§	
Prior Application Filed: May 12, 2000	§	
	§	Examiner: Wilson, A.
Serial No.: Unassigned	§	
	§	
Filed: Herewith	§	
	§	Atty. Docket: MCRO:125--4/FLE
For: METHOD FOR FORMING CONDUCTORS IN SEMICONDUCTOR DEVICES	§	94-0281.04

"EXPRESS MAIL" MAILING LABEL	
NUMBER:	**EV 017 057 185 US**
DATE OF DEPOSIT:	**February 22, 2002**

Pursuant to 37 C.F.R. § 1.10, I hereby certify that I am personally depositing this paper or fee with the U.S. Postal Service, "Express Mail Post Office to Addressee" service on the date indicated above in a sealed envelope (a) having the above-numbered Express Mail label and sufficient postage affixed, and (b) addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

February 22, 2002 — *Date*

Jennifer Presswood — *Jennifer Presswood*

Assistant Commisioner
For Patents
Washington, D.C. 20231

Dear Sir:

PRELIMINARY AMENDMENT

Prior to examination of the above-referenced application, please amend the application as follows:

IN THE SPECIFICATION

Before the first line of the specification, please insert:

-- This application is a divisional of application serial no. 09/570,614, filed on May 12, 2000, and issued as U.S. Patent No. _____, on _____, which is a divisional of application serial no. 08/604,751, filed on February 23, 1996.--

IN THE CLAIMS

Please cancel claims 1-17.

Please add new claims 22-60, as set forth below.

22 (new). The method, as set forth in claim 18, comprising the step of:

forming a plurality of contacts between the first conductive line and the third conductive line, a respective one of the plurality of contacts being formed between respective pairs of memory cells.

23 (new). The method, as set forth in claim 18, wherein the step of providing the first conductive line comprises the step of:

forming a titanium silicide layer over the first conductive line.

24 (new). The method, as set forth in claim 18, wherein the step of forming a plurality of diode access device memory cells comprises the steps of:

for each of the memory cells, forming an access device having a first terminal and a second terminal, the first terminal being in electrical communication with the first conductive line; and

for each of the memory cells, forming a memory element in electrical communication with the second terminal of the access device.

25 (new). The method, as set forth in claim 24, wherein the step of forming an access device comprises the step of:

forming a diode.

26 (new). The method, as set forth in claim 24, wherein the step of forming a memory element comprises the step of:

forming a chalcogenide memory element.

27 (new). The method, as set forth in claim 18, wherein the step of forming a plurality of diode access device memory cells comprises the step of:

forming each of the memory cells to have a width approximately equal to a minimum photolithographic limit.

28 (new). The method, as set forth in claim 27, wherein the step of forming a plurality of diode access device memory cells comprises the step of:

forming pairs of memory cells, each pair being spaced apart by a distance approximately equal to the minimum photolithographic limit.

29 (new). The method, as set forth in claim 22, wherein the step of forming a plurality of contacts comprises the step of:

forming each contact from a doped semiconductive region of the substrate.

30 (new). The method, as set forth in claim 22, wherein the step of forming a plurality of contacts comprises the steps of:

forming dielectric spacers between each pair of memory cells; and

forming each contact between the respective dielectric spacers.

31 (new). The method, as set forth in claim 30, wherein each contact and its respective dielectric spacers have a combined width approximately equal to a minimum photolithographic limit.

32 (new). The method, as set forth in claim 22, wherein the step of forming a third conductive line comprises the step of:

isolating each of the plurality of memory cells from the plurality of contacts.

33 (new). The method, as set forth in claim 32, wherein the step of isolating comprises the step of:

disposing dielectric material on each of the plurality of memory cells.

34 (new). The method, as set forth in claim 33, wherein the step of forming the third conductive line comprises the step of:

forming the third line through tapered holes extending through the dielectric material to the contacts.

35 (new). The method, as set forth in claim 19, comprising the step of:

forming a plurality of contacts between the first conductive line and the third conductive line, a respective one of the plurality of contacts being formed between respective pairs of memory cells.

36 (new). The method, as set forth in claim 19, wherein the step of providing the first conductive line comprises the step of:

forming a titanium silicide layer over the first conductive line.

37 (new). The method, as set forth in claim 19, wherein the step of forming a plurality of memory cells comprises the steps of:

for each of the memory cells, forming an access device having a first terminal and a second terminal, the first terminal being in electrical communication with the first conductive line; and

for each of the memory cells, forming the element in electrical communication with the second terminal of the access device.

38 (new). The method, as set forth in claim 37, wherein the step of forming an access device comprises the step of:

forming a diode.

39 (new). The method, as set forth in claim 37, wherein the step of forming the element comprises the step of:

forming a chalcogenide memory element.

40 (new). The method, as set forth in claim 19, wherein the step of forming a plurality of memory cells comprises the step of:

forming each of the memory cells to have a width approximately equal to a minimum photolithographic limit.

41 (new). The method, as set forth in claim 40, wherein the step of forming a plurality of memory cells comprises the step of:

forming pairs of memory cells, each pair being spaced apart by a distance approximately equal to the minimum photolithographic limit.

42 (new). The method, as set forth in claim 35, wherein the step of forming a plurality of contacts comprises the step of:

forming each contact from a doped semiconductive region of the substrate.

43 (new). The method, as set forth in claim 35, wherein the step of forming a plurality of contacts comprises the steps of:

forming dielectric spacers between each pair of memory cells; and

forming each contact between the respective dielectric spacers.

44 (new). The method, as set forth in claim 43, wherein each contact and its respective dielectric spacers have a combined width approximately equal to a minimum photolithographic limit.

45 (new). The method, as set forth in claim 35, wherein the step of forming a third conductive line comprises the step of:

isolating each of the plurality of memory cells from the plurality of contacts.

46 (new). The method, as set forth in claim 45, wherein the step of isolating comprises the step of:

disposing dielectric material on each of the plurality of memory cells.

47 (new). The method, as set forth in claim 46, wherein the step of forming the third conductive line comprises the step of:

forming the third conductive line through tapered holes extending through the dielectric material to the contacts.

48 (new). The method, as set forth in claim 20, comprising the step of:

forming a plurality of contact plugs between the digit line and the second conductive line, a respective one of the plurality of contact plugs being formed between respective pairs of memory cells.

49 (new). The method, as set forth in claim 20, wherein the step of forming the digit line comprises the step of:

forming a titanium silicide layer over the digit line.

50 (new). The method, as set forth in claim 20, wherein the step of forming a plurality of memory cells comprises the steps of:

for each of the memory cells, forming an access device having a first terminal and a second terminal, the first terminal being in electrical communication with the digit line; and

for each of the memory cells, forming the element in electrical communication with the second terminal of the access device.

51 (new). The method, as set forth in claim 50, wherein the step of forming an access device comprises the step of:

forming a diode.

52 (new). The method, as set forth in claim 50, wherein the step of forming the element comprises the step of:

forming a chalcogenide memory element.

53 (new). The method, as set forth in claim 20, wherein the step of forming a plurality of memory cells comprises the step of:

forming each of the memory cells to have a width approximately equal to a minimum photolithographic limit.

54 (new). The method, as set forth in claim 20, wherein the step of forming a plurality of memory cells comprises the step of:

forming pairs of memory cells, each pair being spaced apart by a distance approximately equal to the minimum photolithographic limit.

55 (new). The method, as set forth in claim 48, wherein the step of forming a plurality of contact plugs comprises the step of:

forming each contact plug from a doped semiconductive region of the substrate.

56 (new). The method, as set forth in claim 48, wherein the step of forming a plurality of contact plugs comprises the steps of:

forming dielectric spacers between each pair of memory cells; and

forming each contact plug between the respective dielectric spacers.

57 (new). The method, as set forth in claim 56, wherein each contact plug and its respective dielectric spacers have a combined width approximately equal to a minimum photolithographic limit.

58 (new). The method, as set forth in claim 48, wherein the step of forming a second conductive line comprises the step of:

isolating each of the plurality of memory cells from the plurality of contact plugs.

59 (new). The method, as set forth in claim 58, wherein the step of isolating comprises the step of:

disposing dielectric material on each of the plurality of memory cells.

60 (new). The method, as set forth in claim 59, wherein the step of forming the second conductive line comprises the step of:

forming the second conductive line through tapered holes extending through the dielectric material to the contact plugs.

REMARKS

Claims 1-17 have been canceled and new claims 22-60 have been added. Consideration of the application as amended is respectfully requested.

If the Examiner believes that a telephonic interview will help speed this application toward issuance, Applicants invite the Examiner to contact the undersigned at (281) 970-4545.

General Authorization for Extensions of Time

In accordance with 37 C.F.R. § 1.136, Applicants hereby provide a general authorization to treat this and any future reply requiring an extension of time as incorporating a request therefor. Furthermore, Applicants authorize the Commissioner to charge the appropriate fee for any extension of time to Deposit Account No. 13-3092; Order No. MCRO:125--4/FLE (94-0281.04).

Respectfully submitted,

Date: February 22, 2002

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